RESEARCH ARTICLE OPEN ACCESS

Dual-Level Adaptive Supply Voltage System with Bandgap Reference MPR for Variation Resilience

Kankanala Pallavi*
*(Department of VLSI Design, JNTU, Hyderabad-75)

ABSTRACT
Nowadays VLSI circuits have become much advanced by overcoming many challenges such as extra power consumption, but circuit aging along with process variations are still challenging the advancements in power efficient VLSI circuits. The aim of this dissertation is to propose the new adaptive technique to efficiently compensate the fine grained variations by addressing the limitations in existing adaption approach. Adaptive supply voltage (ASV) is proved to be one among the top most adaptation approaches in tuning of power performance. Controlling power leakage is the main advantage in using ASV, while delivery overheads along with voltage generation from conventional ASV systems make their application to mitigate fine-grained variations demanding. The main aim of this dissertation is to present a dual level ASV system with band gap reference Miniature programmable regulator (BGRMPR). Reference voltage independent of process and temperature variations can be achieved because of using band gap reference voltage. Another advantage of adapting this approach is because less power is consumed by system when compared to dual-level ASV system with MPR.

Keywords: Band gap reference, aging, Adaptive system, process variation, VLSI circuits.

I. INTRODUCTION

The amount of power used in VLSI designs has been always an issue. VLSI circuits with more than 45nm technologyare adversely effected process variations and aging effects[1]. Extra power would be required to overcome these effects. But this would bring up heat problems. Overdesigning of circuit can be a straight forward way to approach this variation tolerance; thus making sure the circuit is ready for large variations. Power increase to compensate worst cases in overdesign is largely wasted and a need for rebuilding the circuit to use power efficiently is required.

In this paper, a new Adaptive Supply Voltage (ASV) with many critical paths for circuits is proposed. In a typical VLSI circuit design flows, optimisation of circuits is done to reduce power wastage on non-critical path and also reduce the path delay in critical path.Wide range for variation induced timing degradation from a few paths to many paths makes it very hard to implement ASV. Huge overhead on voltage regulators is a drawback for choosing fine grained ASV whereas power wastage is drawback for implementing coarse-grained ASV.

The proposed model solves the above difficulties due to integration of fine grained and coarse-grained ASVs into one design. Power routing disadvantage is avoided in proposed system by voltage tapping technique [6]. In experiments we compare the proposed system with dual-level ASV with MPR. Simulations are carried out on cadence virtuoso tool with considerations of process variations; negative bias temperature instability induced aging affects and stability of the system.

II. EXISTING METHODS AND LITERATURE SURVEY

2.1. Adaptive Body Bias Vs. ASV

Adaptive body bias (ABB) is a most well-known approach that can control transistor threshold voltage in tune with body voltage. ABB lowers transistor threshold voltage if the variation is high to bring the performance back to normal.Similarly, it can increase the threshold voltage to decrease leakage of power. But, still the ASV has many advantages when compared to ABB. ASV can be easily applied to SOI and other circuits when compared with the application of ABB. Limited tuning range is another disadvantage of ASV; ABB impacts only power leakage whereas ASV affects both leakage of power (P_{LEAK}) and dynamic power (P_D). Relationship of power leakage to dynamic or switching power can be

$$P_{LEAK} = I_{LEAK} \star V_{DD}\ P_D = \alpha f C V_{DD}^2 \quad (1)$$

Here,I_{LEAK} represents the cumulative leakage current throughout the circuit, α stands for activity factor, f represents the operating frequency and C is a load capacitance. ASV decreases P_D as well as P_{LEAK} by adjustingV_{DD}. Thus, ASV is proved to be stronger and highly sustainable leverage compared to ABB.

Implementation of ASV is difficult when compared to ease of implementation of ABB. The implementation of ASV generally needs voltage regulators that are either heavy or complicated

whereas tiny circuit like voltage divider can accommodate ABB.

2.2. Dual-level ASV System with MPR

As the name suggests, this system contains both fine grained and coarse grained ASV [6]. Due to combination of both, we have the advantage of solving granularity uncertainty and also allows low overhead of delivery overhead as well as power used in supply voltage generation.

This system is designed based on voltage-island-based designs [2]. In case of the low V_{DD} island, extra power supply is gained by tapping off an intermediate voltageV_f from $V_{DD,H}$ of its adjacent high V_{DD} island. The average level ofV_f value is in between $V_{DD,H}$ and $V_{DD,L}$. $V_f$is built to supply power exclusively to the critical paths in low V_{DD} island [2]. In a rare and temporary case when the dual-ASV system fails to find a nearby $V_{DD.H}$ island for tapping $V_f$because of dynamic voltage control in each voltage island, than system is designed to use global ASV to increase$V_{DD,L}$.

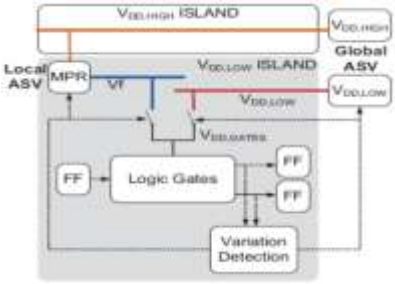

Fig.1. Overview of dual-level ASV

MPR is a designed regulator that down converts high voltage to produce stable dc. This MPR circuit design and operation is similar to that of voltage down converter but for comparatively small load of current. The transistor level Schematic MPR at transistor level is portrayed in Fig. 2.

The MPR is basically composed of three different blocs; voltage divider, voltage follower and a driver transistor. The voltage divider generates reference voltage that is processed further through voltage follower to obtain stable output voltage. The voltage divider circuit is impacted by process variations, thus results in degraded output and poor performance of whole ASV system.

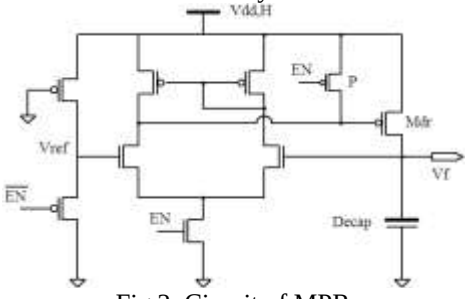

Fig.2. Circuit of MPR

The voltage tapping can be easily achieved by down converting voltagewith the help of voltage regulator. Linear regulator is used as it is simple to integrate on chip and has quick response [3]. This design is programmable due to the EN signal along withcontrol transistor P in Fig.2.The reason for using such simple design with EN signal is that stand power is almost negligible, when MPR is turned off.

Though it is simple design, MPR also works fine for voltage tapping in cases where typical current is nearly 1 mA. The main use of linear regulator [6] is that it stabilizesV_f simultaneously supplying power to dynamic load. The drop in V_f is exponential decrease with the increase in the size ofM_{dr}. To safe guarantee all circuits have drop of less than 5% inV_f, the width of transistor is maintained as 20µm. Both the aging effects (additional V_{th} variation: 3σ = 10%and µ = 10%) and process variations [2] (gate length variation: 3σ = 15% V_{th} variation: 3σ = 20%) are considered through 30 Monte Carlo iterations. The phase margin of 71° confirms MPR design is stable.

III. Basic Blocks Of The Dual-Level Adaptive Supply Voltage System With Bandgap Reference Mpr

Design of bandgap reference MPR is same as MPR except that voltage divider (reference generator) is replaced by a bandgap reference Voltage generator. As mentioned earlier the bandgap reference voltage is independent of process variations as well as temperature.

3.1. Bandgap Reference

The main purpose of using a bandgap reference is to avoid the impact of all external factors like temperature, VDD, process variations; and provide an accurate and stable output. The band gap reference (BGR) circuit [5] is one of the important components in Analogue-to-Digital/Digital-to-analogue converters [3]. These are mostly used in making of radio-frequency and mixed-signal systems. Most of the BGR usesBJT (bipolar junction transistors) to reduce the dependency on temperature.

Fig.3. shows bandgap referencecircuit with MOSFET. The circuit design is just a modification of architecture usedin bipolar transistors. Standard MOS transistors are exclusively used in circuit design. The main objective is to use only one type of transistors in in building the BGR circuit. Despite most of the MOS transistors being parasitic on BJT, the proposed design has only pure MOS transistors [5]. Following equation can extracted from the circuit:

$$V_{DD} = V_{DS_{M1}} + V_{SD_{M4}} + V_{R1} + V_{DS_{M6}}$$
$$V_{DD} = V_{DS_{M2}} + V_{DS_{M5}} + V_{DS_{M7}}$$
$$V_{DD} = V_{DS_{M3}} + V_{R2} + V_{DS_{M8}}$$
$$V_A = V_B \Leftrightarrow V_{R1} + V_{DS_{M6}} = V_{DS_{M7}} \quad (2)$$

M1-M3 are current mirror transistors M1-M3 are current mirrors, M4-M5 force V_A voltage to be same as V_B, this helps in stabilizing the behaviour of circuit with$V_{DD}$and corner variation. R_1andR_2 Resistors are useful in implementing temperature compensation. M6 and M7Transistors produce circuit current and make iteasyfor transistor M8 to preserve voltage with the VDD variation and be stable.

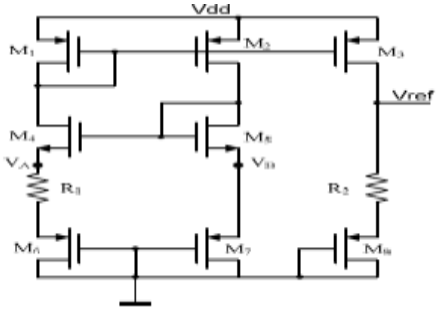

Fig. 3.Bandgap reference with MOS transistors

The output voltage is given by:

$$V_{REF} = V_{GS_{M8}} + R_2 \cdot I \approx \frac{R_2}{R_1} \quad (3)$$

As the resistors value changes from one corner to other, theR_2/R_1 ratio also changes. The correct ratio of R_2/R_1calibration is useful in trimming. Output voltage is generally used in producing voltage reference of any value in any another adjacent circuit before being utilized in DAC, DAC or in any mixed-signal systems.

Simulations are performed for output reference voltage, temperature dependency of output and total power consumed by the band gap reference.

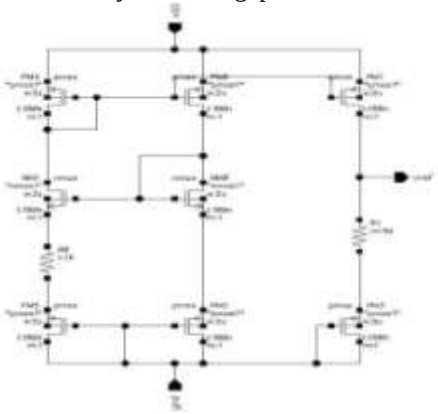

Fig.4.Bandgap Reference

The circuit is simulated for transient response and the output voltage is 0.9V. Output voltage of band gap reference does not change much with temperature.

Fig. 5.Output voltage of Bandgap Reference

Fig.6. Temperature Vs output voltage

Here band gap reference is designed without using BJT's, so power consumption of band gap reference is very less when compare with band gap reference with BJT's. The average power consumed by MOSFET bandgap is 24uW.

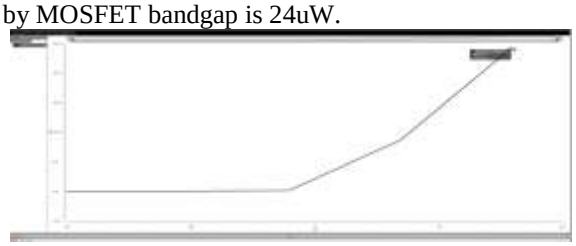

Fig. 7.Average power of bandgap reference

3.2. Voltage Follower

The voltage-follower circuits must be having enough current supply capability with very less output impedance. Thus, large current fluctuations won't show much impact on output voltage. A single-stage voltage follower represented in Fig.8.isthe VDC in memory chip Application.100mA is the maximum value ofI_L.

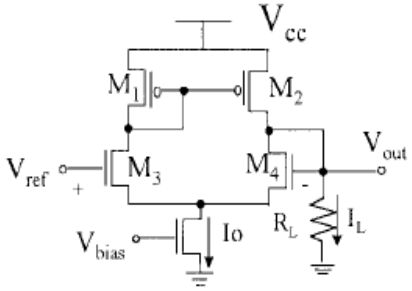

Fig.8. Single-stage voltage follower

3.3. Driver transistor/Output driver

A transistor of comparatively large size is connected at output to enlarge drivability of VDC.

3.4. An alternative aging sensor

Stability checking is the main idea behind the design of alternative aging sensor [4]. The concept of

this is to pre-sample the combinational logic output (using a delay element)and compare with the actual output value (with the help of XOR gate). Delay element 'Tg' is same as guard band interval. If guardband is violated because of aging, then 2 sample values noted will vary and XOR gate will report the difference.

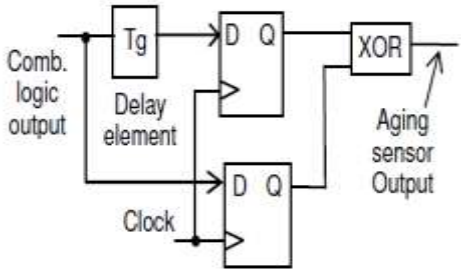

Fig. 9. Alternative aging sensor design

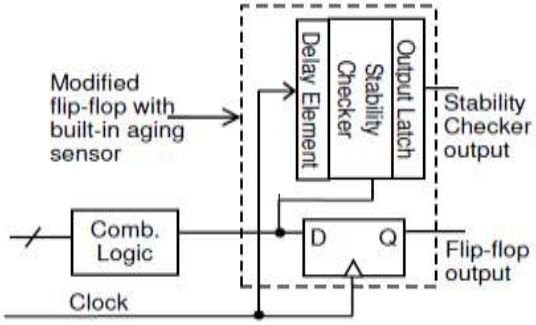

Fig.10. Flip-flop with built-in aging sensor

3.4.1 Delay element

The global input signal/Monitor may be taken from scan enable signal. If Monitor = 1, aging monitoring will be turned on and leading to the delayed version, Clock_b. If Monitor = 0, aging monitoring will be turned off and the delay element would produce 1. This would also reduce power consumption by the delay element. But, we should make sure that source-gate junctions of PMOS transistors utilized in producing guard band interval should not be forward biased.

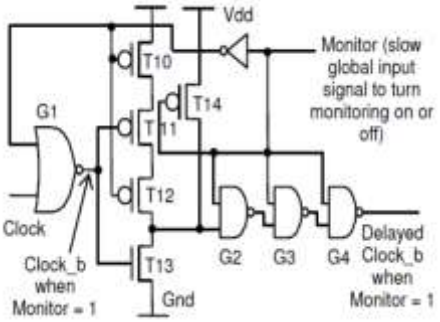

Fig.11.Design of delay element.

3.4.2. Stability checker

The design of a stability checker is shown in Fig.12.andthe corresponding waveforms in Fig.13. In the initial stages of clock cycle, when Clock= 1 (Clock_b= 0), T1 and T5 PMOS transistorsare on (i.e. T3 and T7 NMOS transistors are off), and therefore, *Out* = 0 (stability checker output). This is termed asprecharge phaseof stability checker[4].

As shown in Fig.11.delay element (Delay)induces a delay of 'Tclk/2 – Tg' (50% duty cycle is assumed inClock). This indicates that T3 and T4 transistors are ON along with T7 and T8 during Guard band interval (This is evaluate phase). During this phase, T1 and T5 PMOS transistors are off. Stability Checker output Out = 1. If combinational logic output OUT changes from 1 to 0 or vice versa at the time of guard band interval (once or multiple times), than we can assume guard band is violated.

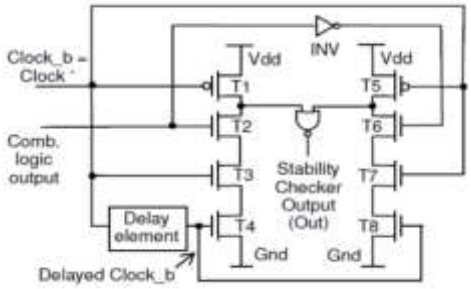

Fig. 12.Stability Checker design

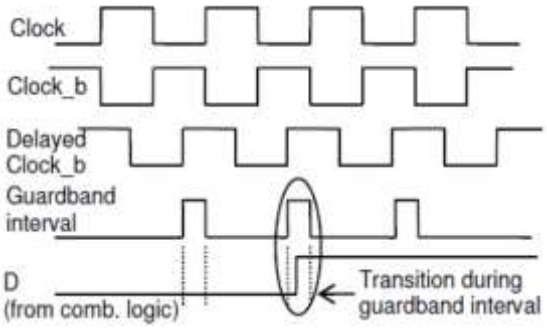

Fig.13.Timing Diagram for sensor

IV. IMPLEMENTATION OF DUAL-LEVEL ADAPTIVE SUPPLY VOLTAGE SYSTEM WITH BANDGAP REFERENCE MPR

Band Gap reference MPR is also a programmable regulator. BGRMPR is turned off, if EN is low. With the application of EN signal, we don't have to worry regarding standby current as in conventional regulator designs. Standby power is almost negligible (around 72pW) when compared to the power of whole circuit. The efficiency of each BGRMPR can be increased, when the level of $V_{DD,H}$ is as near to V_f as possible in near-by voltage islands, as the efficiency of the linear regulator increases with the low-dropout voltage. When it is ON, BGRMPR consumes around 100uW, hence, BGRMPR consumes low power when the power of whole

circuit is considered. As the design is simple, it works comfortable for voltage tapping (Typical current around 1 mA). In this case, $V_{DD,H}$= 1.1V, $V_{DD,L}$=0.8 V and V_f= 0.9 V.

Linear regulator helps in stabilizing V_f simultaneously supply power to dynamic load. We notice that the impact on voltage drop ofV_f. This is very important to the predictability andperformance of logic circuits. Exponential decrease in V_f drops is observed with the size increase ofM_{dr}.Transistor width of M_{dr} is setup as 20μm in order to ensure all circuits under the variations have V_f drops less than 5%,. The phase margin of 85° confirms the proposed BGRMPR design is stable. The transistor level schematic of bandgap MPR is shown in Fig.14.

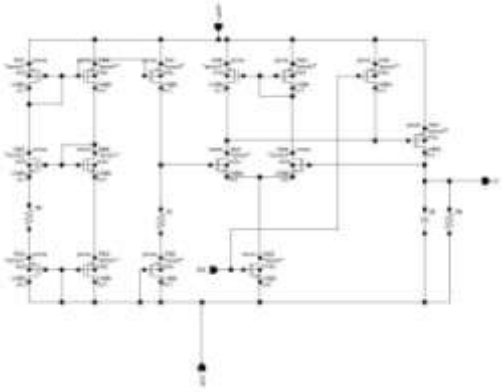

Fig.14. Circuit of BGRMPR

4.1. Progressive voltage enhancement

In this section, we introduce on utilizing the 2 dynamic voltage levels for the purpose of variation resilience in various scenarios [7]:Starting from single path to multi paths of variation assertions. Two different ways are proposed underneath for connections withvoltage tapping output V_f .

1) Single path block – selective connection:One BGRMPR design is connected to single-path blocks (less than 3)using switches (sleep transistors). However, only connections to maximum of two blocks could be turned on simultaneously because of limited capacity of BGRMPR to supply power. With this kind of connections, BGRMPR selectively focuses its capacity on 1 or 2 paths to supply additional power to compensate variation.
2) Multipath block – direct connection: This block is a combination of logic gates that are shared by multiple(equal or more than 3) critical paths. No switches are used while connecting BGRMPR directly with multipath block.It should be noted that direct connection [6] need not mean BGRMPR powers multi-block, as BGRMPR can be turned off by EN signal.All the shared paths will be provided with additional power through connection for the compensation of variation.

Numbers of gates are equal in every block regardless of multipath or single path and hence, single path block supplies more power to one path than multipath. As multiple path block has to share power with several paths during sparse variations.

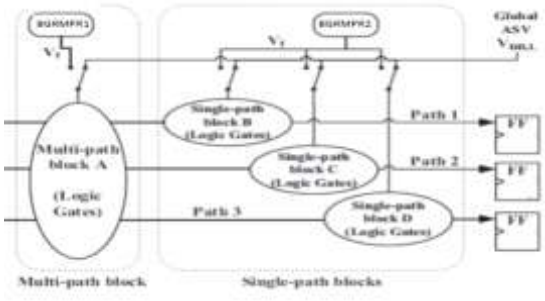

Fig.15. Illustration for progressive voltage enhancement

The proposed design of dual-ASV system is common practice and well-studied in the context of standard design flow of VLSI-CAD.

V. SIMULATION RESULTS

Schematic design and simulations are done on cadence virtuoso tool of 180nm.

5.1 MPR

Fig.16. shows transistor level schematic of MPR. MPR is simulated for output voltage, transient response, output voltage variation with respect to temperature and total power consumed by the MPR.

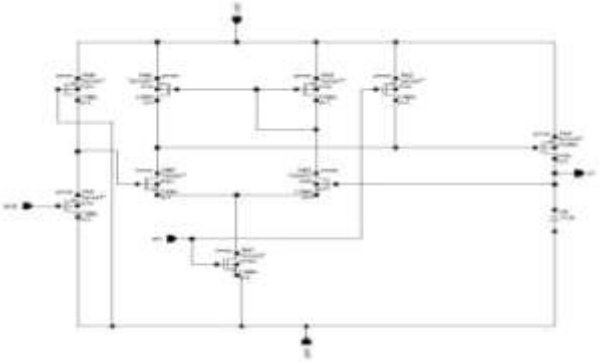

Fig.16. Schematic of MPR

Fig.17. shows the output voltage of MPR. The output voltage of MPR is 0.896V. The transient analysis shows that the output voltage of MPR is 0.896V and it is a dc voltage.

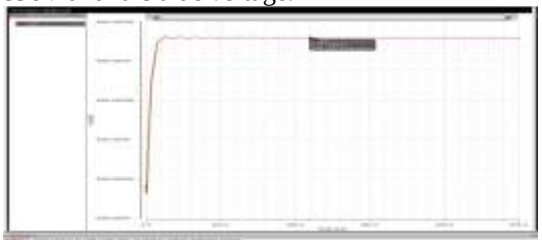

Fig. 17.Output voltage (V_f) of MPR

Fig.18. shows the average power consumed by MPR. The total power consumption of MPR is 125uW. It is negligible when compared to total system power. Thus, MPR is not a power burden for dual-level ASV system.

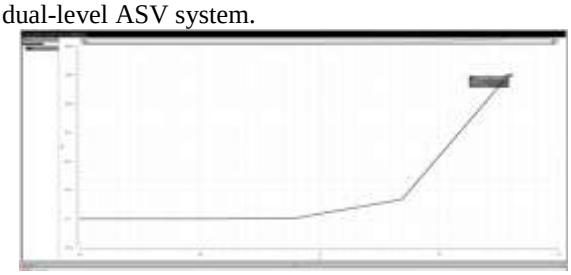

Fig.18. Average power of MPR

Fig.19. shows the temperature dependence of MPR. This proves that the output voltage of MPR is decreased as temperature is increased.

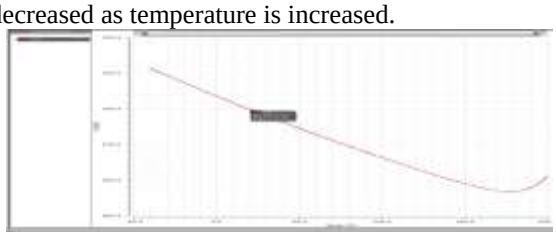

Fig.19. Temperature Vs output voltage of MPR

As shown in Fig. 19. MPR output gets degraded with temperature i.e. MPR cannot be operated at higher temperatures.

5.2. BGRMPR

Fig.20. shows transistor level schematic of band gap Reference MPR. The important parameters of BGRMPR are output voltage, transient analysis, output dependency on temperature against total power consumed by BGRMPR and the circuit stability that is observed while analysing the phase margin of BGRMPR. Transient analysis of BGRMPR is shown in Fig.21. From the transient analysis, it is known that the output voltage of BGRMPR as 0.896V which equal to MPR output voltage. As shown in Fig.20.one capacitor is connected at the output which is utilised to suppress the supply noise. Load current can manually changeby changing the resistor that is connected at output.

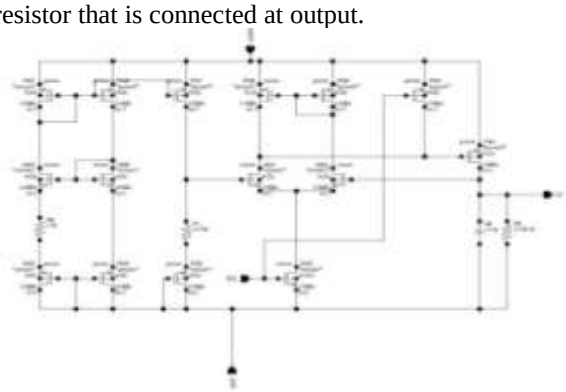

Fig.20. Schematic of BGRMPR

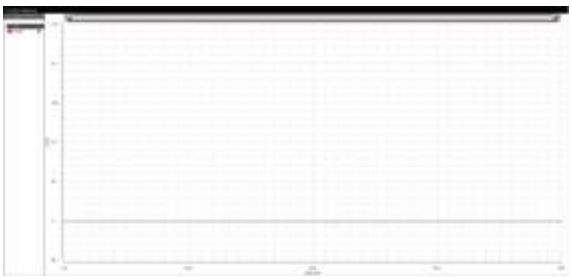

Fig.21. Output of BGRMPR

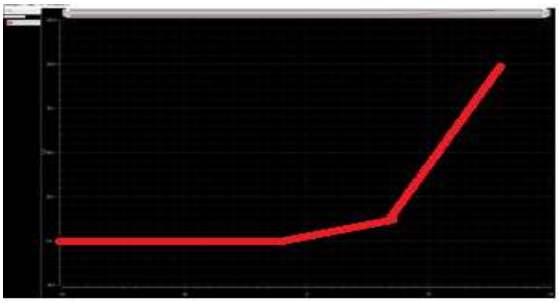

Fig.22. Average power of BGRMPR

Fig.22 shows the average power consumption by BGRMPR. The average power consumed by BGRMPR is 100uW. Fig.5.15 shows that BGRMPR is temperature independent.

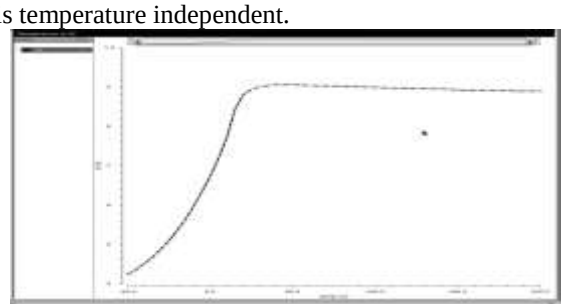

Fig.23. Temperature Vs. output voltage

As shown in Fig.23.the output voltage of BGRMPR does not vary with temperature. This is the main advantage of using the BGRMPR over MPR. MPR output decreases as temperature increases. Phase margin of BGRMPR is shown in Fig.24.

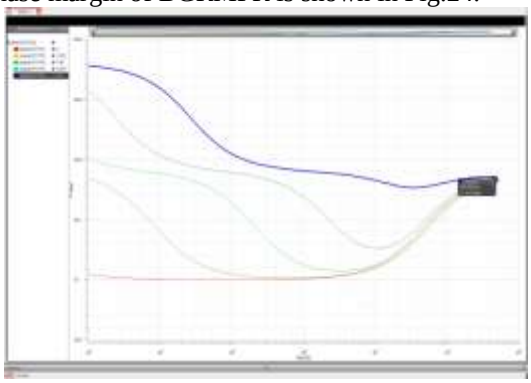

Fig.24. Phase margin of BGRMPR

The phase margin of BGRMPR 85^{o} is confirms that the BGRMPR is stable. Therefore the Band gap

Reference Miniature Programmable regulator is independent of both temperature and process variations.

5.3. Dual-level ASV system

As discussed earlier, the dual-level ASV system is made up of two voltage levels; $V_{DD,H}$ and$V_{DD,L}$. $V_f$an intermediate voltage would be produced by tapping off $V_{DD,H}$. By default all the combinational circuits are connected to $V_{DD,L}$. If the combinational circuit has delay variation, than sensor that is connected at every output will make transition from low to high. Sleep transistors are utilised in connecting intermediate voltage $V_f$and circuits that are showing delay variation. When all circuits are flagged for delay variation, then all of them are connected to$V_{DD,H}$. This situation can be termed as multipath connection. As the delay is in nanoseconds, simulations are also performed in nanoseconds. Fig.25. Shows the Default connections of dual-level ASV

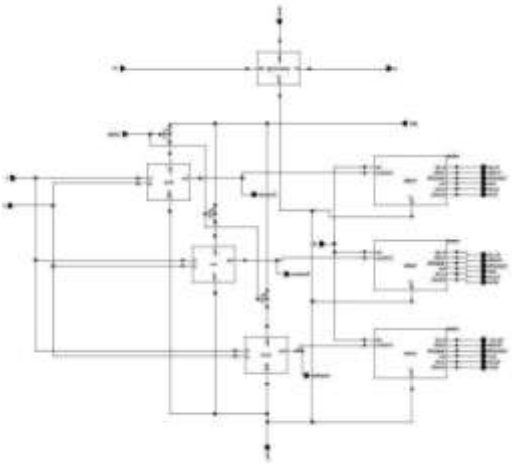

Fig.25. Default connections of Dual-level ASV

When circuits are connected to $V_{DD,L}$by default all combinational circuits will get power supply from $V_{DD,L}$.Fig.26. Shows output wave forms of $V_{DD,L}$driving.

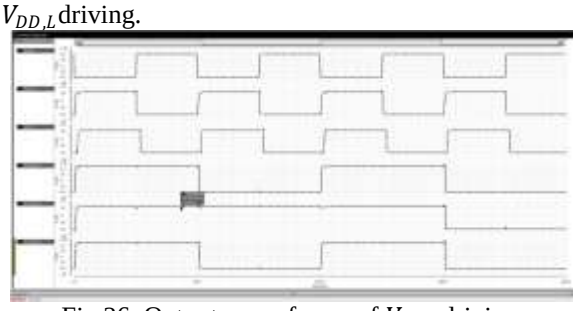

Fig.26. Output wave forms of $V_{DD,L}$driving

If any circuit flags delay variation that circuit will be connected to the output voltage of BGRMPR.

The circuit connections toV_f is shown in Fig.27and its output wave forms are shown in Fig.28.

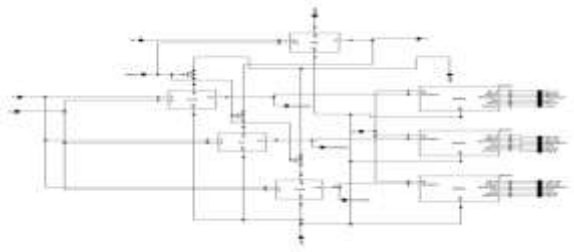

Fig.27.V_f connection to delay variation circuit

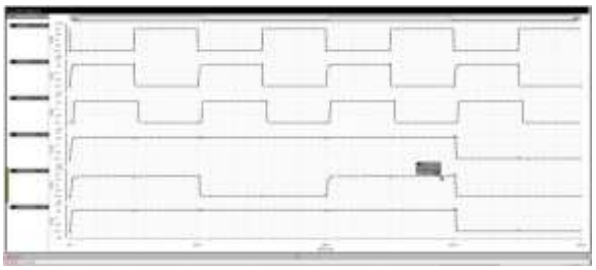

Fig.28. Output of BGRMPR driving the delayed circuit

When all circuits are flagged for delay variation, then all of them are connected to$V_{DD,H}$. Fig.29. shows $V_{DD,H}$ connection to all circuits and Fig.30.shows the output waveforms of $V_{DD,H}$ connection.

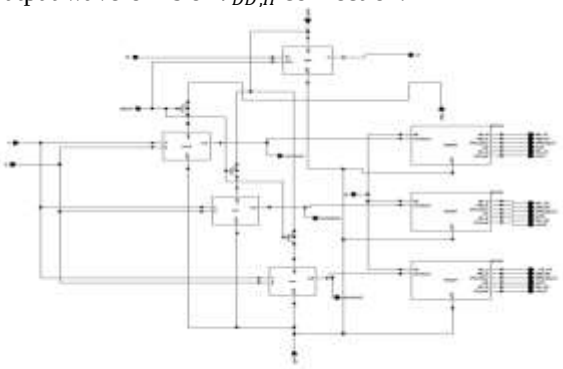

Fig.29.$V_{DD,H}$ connection of Dual-level ASV system

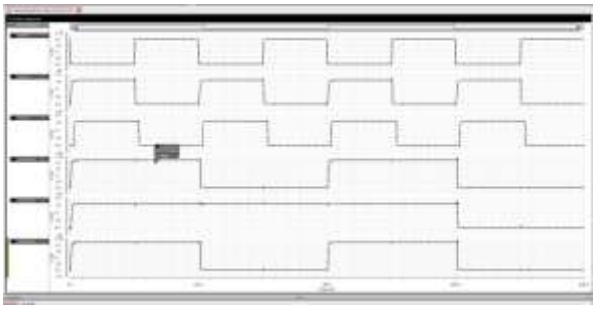

Fig.30 output of $V_{DD,H}$connection of Dual-level ASV system

The total power consumed by the Dual-level ASV system is shown in Fig.31. Total power dissipated to Dual-level ASV system is 260uW.

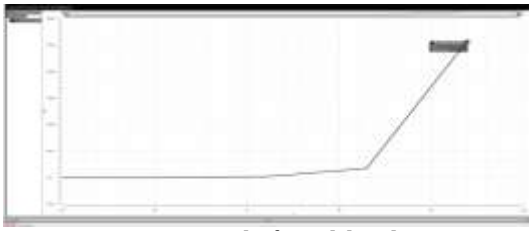

Fig.31. Power consumed of Dual-level ASV system with BGRMPR

Fig.32. shows that the power consumption of Dual-level ASV system when it uses MPR for driving delay variation circuits.

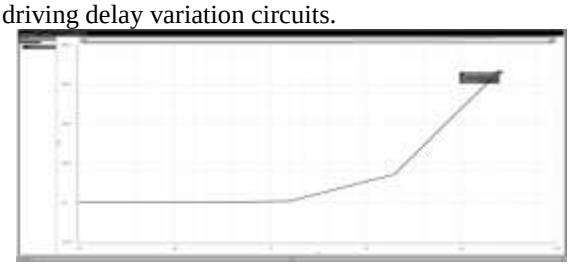

Fig.32.Power consumed by Dual-level ASV system with MPR

From Fig.31 and Fig.32 it is clear that the average power consumed by BGRMPR Dual-level ASV system is less when compare to MPR Dual-level ASV system.

Table. I.
Comparison of Dual-level ASV system with MPR and BGRMPR**.**

Variable	Dual-level ASV with MPR	Dual-level ASV with BGRMPR
$V_{DD,H}$	1.1V	1.1V
$V_{DD,L}$	0.8V	0.8V
V_f	0.896V	0.896V
Power	334uW	260uW

Table. II.
Final results of the all techniques

Technique	Author	Techno logy	Power	Year
Dual-level ASV with BGRMPR	--	180nm	260uW	2015
Dual-level ASV with MPR	Kyu-Nam Shim	180nm	334uW	2013
Dual-static supply	K. Agarwal and K. Nowka	180nm	NA	2007
Online adjustable buffer	A. B. Kahng, S. Reda, and P. Sharma	90nm	300uW	2007

Hence, it is proved that temperature changes and process variations doesn't impact the performance of BGRMPR. Thus, the total power wastage of circuit is less, when compared to any other adaptive power supply models.

VI. CONCLUSIONS AND FUTURE SCOPE

As the technology advances in VLSI design, challenges are increasing due to variations of fine grained nature and aging of circuits. In this paper, proposed design can overcome these challenges to some extent and increase the efficiency of circuit. Limitations in existing models like ABB and conventional ASV can be overcome by in building BGRMPR into ASV. Band Gap reference MPR is proposed in building the ASV system to achieve power saving by overcoming process variations. As discussed, circuit aging can also be addressed by using the proposed design.

REFERENCES

[1]. S. Borkar, "Designing reliable systems from unreliable components: The challenges of transistor variability and degradation, "*IEEE Micro*, 25(6), 2005, pp. 10–16.

[2]. D. E. Lackey, P. S. Zuchowski, T. R. Bednar, D. W. Stout, S. W. Gould, and J. M. Cohn, "Managing power and performance for system-on-chip designs using voltage island," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design*, 2002, 195–202.

[3]. S.-J. Jou and T.-L.Chen, "On-chip voltage down converter for low power digital system," *IEEE Trans. Circuits Syst. II, Analog Digital Signal Process, 45(5)*, 1998, 617–625.

[4]. M. Agarwal, B. C. Paul, M. Zhang, and S. Mitra, "Circuit failure prediction and its application to transistor aging," in *Proc. IEEE VLSI Test Symp.*, 2007, 277–286.

[5]. "A Bandgap Voltage Reference with Only MOS Transistors" by Antonio Ribeiro, Ricardo Gama, Tiago Costa, Rui Neves, Nuno Horta Paulo Pereira

[6]. "Dual-level Adaptive Supply Voltage System for Variation resilience" by Kyu-Nam Shim, Jiang Hu, and Jose Silva-Martinez.

[7]. E. Talpesand D. Marculescu, "Toward a multiple clock/voltage island design style for power-aware processors," *IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst., 13(5)*, 2005, 591–603.